REMARKS

Claims 1-16 and 18-24 are all the claims presently pending in the application, and claims 1-9 and 11-16 stand rejected on prior art grounds. Applicant hereby affirms the election, made during a telephone conversation with the Examiner on September 30, 2002, of Group I, (e.g. directed to a method of forming an interconnect on a semiconductor device substrate) upon which at least claims 1-16 are readable, without traverse. Applicant reserves the opportunity to file a Divisional Application for the non-elected invention later.

Claims 6, 10, and 15 were amended to overcome informalities cited by the Examiner, and claims 18-23 are added to claim additional features of the invention. No new matter is added to the amended claims or new claims. The claims are amended to merely clarify the subject matter of the claims and not to narrow the scope of the claims in order to overcome the prior art or for any statutory purposes of patentability. Notwithstanding any claim amendments of the present Amendment or those amendments that may be made during prosecution, Applicant's intent is to encompass equivalents of all claim elements. Attached hereto is a marked up version of the changes made in the specification and/or claims by the current Amendment.

With respect to the prior art rejections, claims 1-3, 5, 8-9, 12-14, and 16 stand rejected under 35 U.S.C. § 102(b) as anticipated by Shoda (U.S. Patent No. 5,529,953).

Claims 4 and 11 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shoda in view of Liu, et al. (U.S. Patent No. 6,284,642).

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Shoda in view of S. Wolf (*Silicon Processing for the VLSI Era*, Vol. 2, p. 194).

Claim 15 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Shoda.

The prior art rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

Applicant's invention, as disclosed and defined in claim 1, is directed to a method of forming an interconnect on a semiconductor substrate that includes forming a relatively narrow first structure in a dielectric formed on a semiconductor substrate, forming a relatively wider second structure in the dielectric formed on the semiconductor substrate, forming a liner in the first and second structures such that the first structure is substantially filled and the second substrate is substantially unfilled, and forming a metallization over the liner to completely fill the second structure.

The conventional method typically attempts to fill substantially both small and large contact structures with copper, thereby requiring additional and costly processing. For example, it is difficult to adequately line contacts for copper filling at contact dimensions below 280 nm and to line contacts reliably below contact opening sizes of less than 320 nm. The conventional methods present a major challenge to dynamic random access memory back-end-of-line (DRAM BEOL) processing when applying copper to line contacts.

The claimed method, on the other hand, forms a liner in an exemplary first relatively narrow contact structure and an exemplary second relatively wider contact structure that is formed on a semiconductor substrate, and subsequently forms a metallization over the liner to completely fill the second structure. This is important because small contacts on a semiconductor

device can be filled with a highly reliable material and wider metal lines, or slots, can be filled with copper.

Thus, advantages to the invention include filling the substantially smaller areas and structures with CVD metal, and the wider areas and structures with copper metallization.

II. THE 35 U.S.C. §112, SECOND PARAGRAPH, REJECTION

Claim 10 stands rejected under 35 U.S.C. 112, second paragraph. Applicant respectfully submits that claim 10 is amended to overcome informalities and requests the Examiner to reconsider and withdraw the rejection.

III. THE PRIOR ART REJECTIONS

THE 35 U.S.C. § 102(b) REJECTION BASED ON SHODA

The Examiner alleges claims 1-3, 5, 8, 9, 12-14, and 16 are anticipated under by Shoda. Applicant submits, however, that there are elements of the claimed invention which are not found in Shoda. Shoda discloses selecting the appropriate conductive materials used to fill an interconnect groove and a contact hole that are formed within a dielectric material, thereby creating a dual damascene structure. (Shoda, col. 3, lines 40-50). Conductive materials, such as tungsten, are selected for forming conductive layers such that the incubation time for depositing a conductive layer within the contact hole is shorter than the incubation period for depositing a conductive layer within the relatively larger groove (Shoda, col. 4, lines 15-20).

As is clear, applicant submits that Shoda teaches different objectives and matters as the

present application and therefore does not anticipate or for that matter render obvious the claimed invention. The inventive method of the present invention, as defined exemplarily in claim 1, recites at least the features of "forming a liner in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and forming a metallization over said liner to completely fill said second structure." Shoda does not teach or suggest the method of forming a liner over first and second structures, and then forming a layer (e.g. a metallization) over the second liner (and hence over both structures).

Further, independent claim 5 recites at least the features of "forming a contact including a slot, in a dielectric on a semiconductor substrate; forming troughs into the dielectric . . . depositing a conducting material on the dielectric" . . . and "depositing a metal over the conducting material to completely fill the slot and troughs."

Independent claim 16 also recites at least the features "depositing a conducting material on the dielectric . . ." and "depositing a metal over the conducting material to completely fill the slot and troughs." None of the features recited in claim 5 or claim 6 features is taught or suggested by Shoda.

Shoda is directed to forming conductive layers on the bottom portions of a contact hole and groove within the dielectric and subsequently filling both the contact hole and trench with the same conductive material (e.g., tungsten).

Shoda relies upon the difference in the incubation times of the conductive material that is deposited upon the different conductive layers to selectively fill each of the contact hole and groove with the same conductive material (Shoda, col. 4, lines 27-37). Therefore, Shoda teaches

the use of manipulating the incubation times of the conductive material (e.g. tungsten) to fill contact holes and grooves within a dielectric.

The claimed invention does not rely on the incubation times of a conductive material to form the exemplary structures. Instead, in an exemplary embodiment, a dual damascene interconnection is formed on a wafer preferably by first etching contacts 101 and slots 102 into a dielectric 102. Secondly, troughs 104 are etched into the dielectric 103. Next, a reliable conducting material, such as chemical vapor-deposited metal (e.g. tungsten) is deposited with the material thickness adjusted to substantially fill the relatively small contacts 101. A conducting metal or material (e.g. copper) is then deposited over the tungsten to completely fill the relatively wider lines (e.g. the slots 102 and troughs 104). In the next stage, the copper is polished back either to the contact fill material (e.g. tungsten) or both the copper and tungsten are simultaneously polished to the dielectric. The tungsten is then selectively removed from the wafer by etching or CMP (Application, p. 5, line 7 to p. 6, line 14).

Therefore, it is clear that Shoda does not teach or suggest the novel method of forming a liner in relatively narrow and wider structures in a dielectric "such that the first structure is filled and the second structure is substantially unfilled; and forming a metallization over said liner to completely fill said second structure" as recited in claim 1.

Further, there is no teaching or suggestion in Shoda of depositing a conducting material on the dielectric, depositing a metal layer over the conducting material, and then removing the materials back to the dielectric. Accordingly, Shoda does not teach or suggest "removing the metal either to the conducting material or both the metal and the conducting material

simultaneously back to the dielectric; and selectively removing the conducting material," as recited in independent claims 5 and 16.

For at least the reasons outlined above, Applicant respectfully submits that Shoda fails to teach or suggest every feature of claims 1, 5, and 16. Accordingly, Shoda fails to anticipate or render obvious the subject matter of claim 1 and claims 2-4, which depend from claim 1; the subject matter of claim 5 and claims 7-9 and 12-15,which depend from claim 5; and claim 16. Withdrawal of the rejection of claims 1-3, 5, 8, 9, 12-14, and 16 under 35 U.S.C. § 102(b) is respectfully solicited.

Hence, turning to the clear language of claim 1, there is no teaching or suggestion of *"forming a liner in said first and second structures such that said first structure is substantially filled and said second structure is substantially unfilled; and forming a metallization over said liner to completely fill said second structure,"* nor is there teaching or suggestion of *"depositing a conducting material on the dielectric; depositing a metal over the conducting material to completely fill the slot and troughs; removing the metal either to the conducting material or both the metal and the conducting material simultaneously back to the dielectric; and selectively removing the conducting material,"* as recited in independent claims 5 and 16.

For the reasons stated above, the claimed invention is fully patentable over the cited references. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

THE 35 U.S.C. § 103(a) REJECTION BASED ON SHODA

Regarding the 35 U.S.C. 103(a) rejection of claim 15, as being unpatentable over Shoda, the deficiencies of Shoda have been discussed above. Modifying Shoda to duplicate the deposition of dielectric films and metal layers on the resulting structure fails to make up for Shoda's deficiencies.

That is, turning to the clear language of claim 15, there is no teaching or suggestion of "*repeating said depositing a conducting material; and repeating said depositing a metal over the conducting material, thereby depositing subsequent said conducting material and said metal on the resulting structure*".

Further, Applicant submits that claim 15 is patentable not only by virtue of its dependency from claim 5 but also by the additional limitation it recites.

Therefore, the subject matter of claim 15 is fully patentable over the cited reference, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

THE LUI ET AL REFERENCE

Regarding the 35 U.S.C. 103(a) rejection of claims 4 and 11 as being unpatentable over Shoda in view of Liu et al, the deficiencies of Shoda have been discussed above. Liu et al clearly fails to make up for Shoda's deficiencies.

That is, turning to the clear language of claim 4, there is no teaching or suggestion of the claim 1 method for forming an interconnect on a semiconductor substrate, "*wherein said metallization comprises copper.*" Further, there is no teaching or suggestion of the claim 5

method for forming an interconnect on a semiconductor substrate, *"wherein said metal comprises copper,"* as recited in claim 11.

Applicant submits that claims 4 and 11 are patentable not only by virtue of their dependency from their respective independent claims but also by the additional limitations they recite. Therefore, the subject matter of claims 4 and 11 are fully patentable over the cited references, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

THE WOLF REFERENCE

Regarding the 35 U.S.C. 103(a) rejection of claims 6 and 7 as being unpatentable over Shoda in view of S. Wolf, the deficiencies of Shoda have been discussed above. Wolf clearly fails to make up for Shoda's deficiencies.

That is, turning to the clear language of claim 6, there is no teaching or suggestion of the claim 5 method of forming an interconnect on a semiconductor substrate *"wherein said dielectric comprises one of tetraethylorthosilicate (TEOS) oxide, silane oxide, and another low K polymer dielectric."* Further, there is no teaching or suggestion of the method of claim 6, *"wherein said contacts comprise contacts formed between first and second metal levels formed on the semiconductor substrate,"* as recited in claim 7.

Applicant submits that claims 6 and 7 are patentable not only by virtue of their dependency from their respective independent claims but also by the additional limitations they recite. Therefore, the subject matter of claims 6 and 7 are fully patentable over the cited references, and the Examiner is respectfully requested to reconsider and withdraw this rejection.

Therefore, Applicant respectfully submits that these references would not have been combined as alleged by the Examiner and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

IV. INFORMAL MATTERS AND CONCLUSION

Regarding the drawings, Applicant submits that Figures 4 and 5 show prior and subsequent views of the selective removal process in claims 5 and 13. Claims 5 and 13 recite "selectively removing said conductive material." This process is described in the exemplary embodiment on page 6, lines 10-14 of the Application, reciting "as shown in Figure 5, the tungsten is selectively removed, either by a selective etch, or by a selective CMP . . . [t]hus, Figure 5 illustrates the wafer cross-section after selective removal of the tungsten, either by selective etch or CMP." Thus, Figure 4 illustrates a tungsten layer at the wafer surface prior to selective removal. Figure 5 illustrates a view subsequent to the selective removal of the conductive material (e.g. tungsten), thereby creating a new surface area of the wafer. Therefore, the features of selectively removing the conductive material in claims 5 and 13 are fully illustrated, and the Examiner is respectfully requested to reconsider and withdraw this objection.

Regarding the objection to claim 15, the claim recites the method elements of "repeating said depositing a conducting material and repeating said depositing a metal over the conducting material." These elements recite the repeated processes referenced in independent claim 5 to further form the resulting structure and are accordingly fully illustrated in the respective Figures 1-5. Therefore, the features of repeating deposits of conducting material and metal in claim 15

are fully illustrated, and the Examiner is respectfully requested to reconsider and withdraw this objection.

Claim 6 has been amended to overcome the Examiner's objection. Specifically, in claim 6 the terms "TEOS and silane" were replaced with "TEOS oxide" and "silane oxide," respectively.

In view of the foregoing, Applicant submits that claims 1-16 and 18-24, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to withdraw the rejections and pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner may contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 1/23/03

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 6 and 10 have been amended, as follows:

6. (Amended) The method of claim 5, wherein said dielectric comprises one of tetraethylorthosilicate (TEOS) oxide, silane oxide, and another low K polymer dielectric.

10. (Amended) The method of claim 5, wherein a thickness of the conducting material is adjusted so as to completely fill the [relatively small contacts] slot.

15. (Amended) The method of claim 5, further comprising:

repeating said depositing a conducting material; and

repeating said depositing a metal over the conducting material, thereby depositing subsequent [dielectric films] said conducting material and said metal [layers] on the resulting structure.